

High precision voltage regulator

Features

- Input voltage up to 40 V
- Output voltage adjustable from 2 to 37 V
- Positive or negative supply operation
- Series, shunt, switching or floating operation
- Output current to 150 mA without external pass transistor
- Adjustable current limiting

Description

The LM723 is a monolithic integrated programmable voltage regulator, assembled in 14-lead dual in-line plastic package. The circuit provides internal current limiting. When the output current exceeds 150 mA an external NPN or PNP pass element may be used. Provisions are made for adjustable current limiting and remote shut-down.

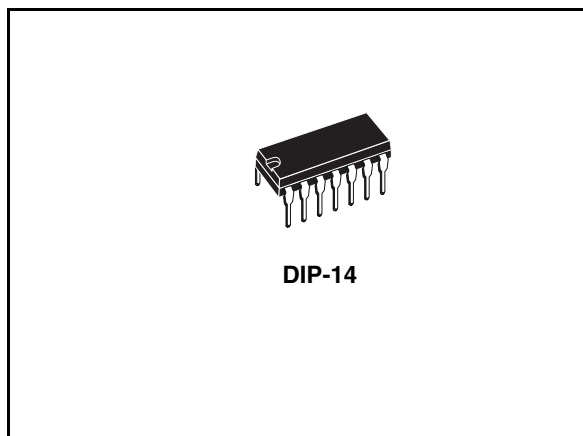


Table 1. Device summary

Order code	Package
LM723N	DIP-14
LM723CN	DIP-14

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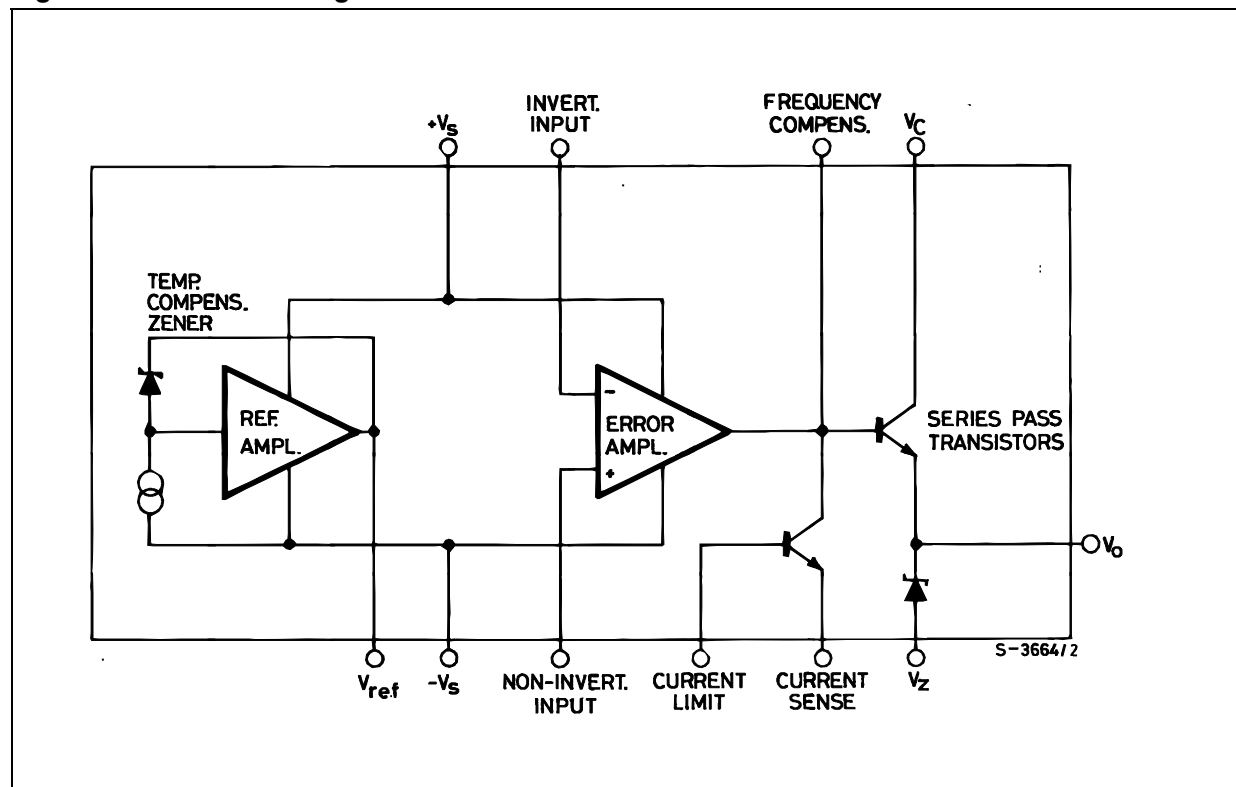
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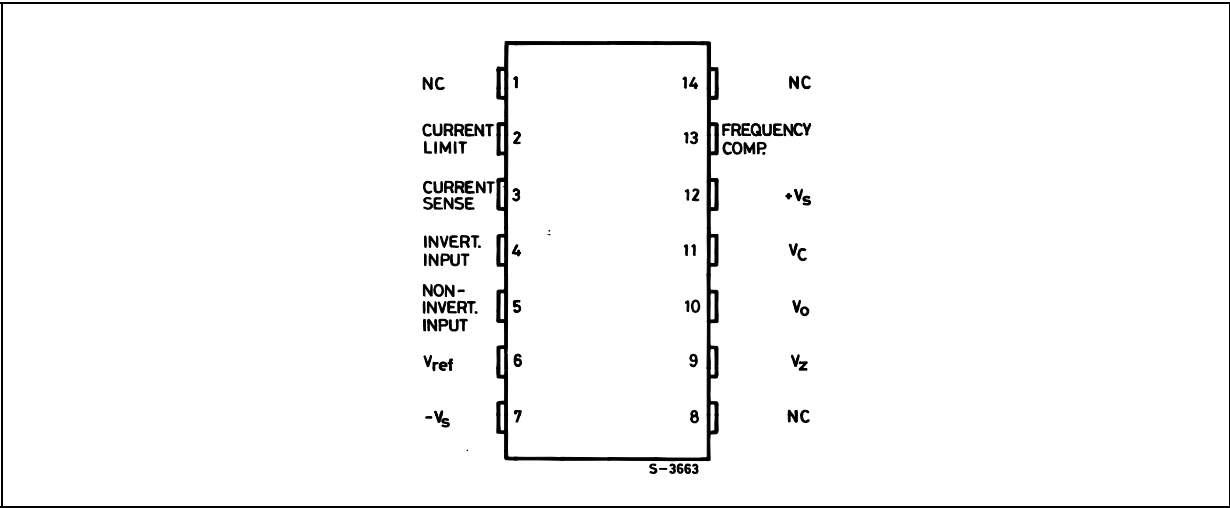
1 Diagram

Figure 1. Schematic diagram



2 Pin configuration

Figure 2. Pin connections (top view)



3 Maximum ratings

Table 2. Absolute maximum ratings

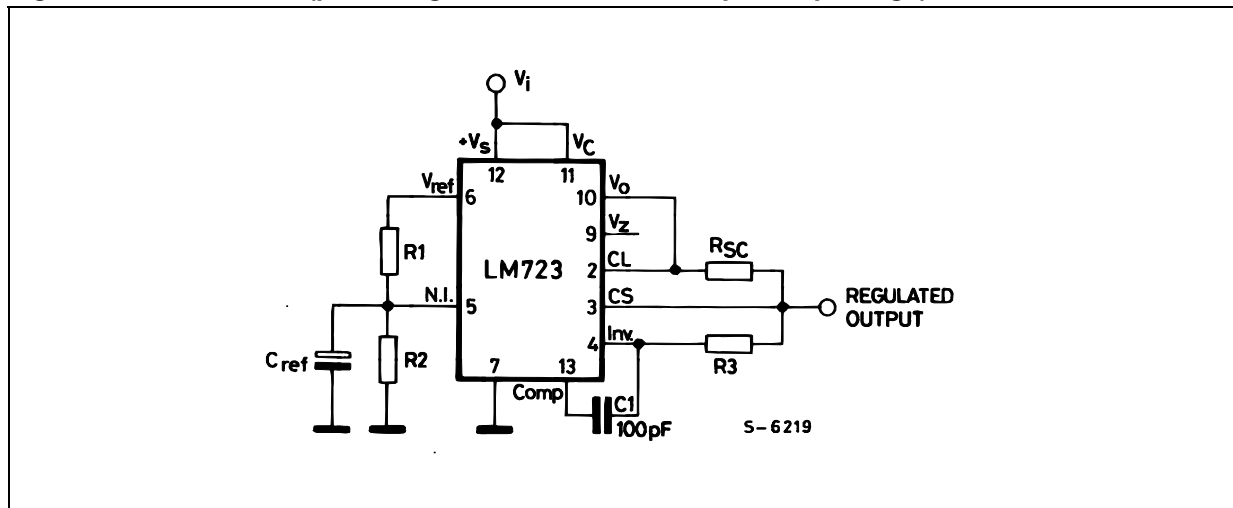
Symbol	Parameter	Value		Unit
		LM723	LM723C	
V_I	DC input voltage	40	40	V
ΔV_{I-O}	Dropout voltage	40	40	V
I_O	Output current	150	150	mA
I_{REF}	Current from V_{REF}	15	25	mA
T_{OP}	Operating Temperature	-55 to 125	0 to 70	°C
T_{STG}	Storage Temperature	-65 to 150	-65 to 150	°C
T_J	Junction Temperature	150	125	°C

Table 3. Thermal data

Symbol	Parameter	DIP14	Unit
R_{thJA}	Thermal resistance junction-ambient Max	200	°C/W

4 Circuit

Figure 3. Test circuit (pin configuration relative to the plastic package)



Note: $V_I = 12\text{ V}$; $V_O = 5\text{ V}$; $I_O = 1\text{ mA}$; $R_1/R_2 \leq 10\text{ k}\Omega$

5 Electrical characteristics

Table 4. Electrical characteristics for LM723 (refer to the test circuits, $T_A = 25^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$\Delta V_O / \Delta V_I$	Line regulation	$V_I = 12 \text{ to } 15 \text{ V}$			0.01	0.1	%
		$V_I = 12 \text{ to } 40 \text{ V}$			0.02	0.2	
		$V_I = 12 \text{ to } 15 \text{ V}, T_A = -55 \text{ to } 125^\circ\text{C}$				0.3	
$\Delta V_O / V_O$	Load regulation	$I_O = 1 \text{ to } 50 \text{ mA}$			0.03	0.15	%
		$I_O = 1 \text{ to } 10 \text{ mA}, T_A = -55 \text{ to } 125^\circ\text{C}$				0.6	
V_{REF}	Reference voltage	$I_{REF} = 160 \mu\text{A}$		6.95	7.15	7.35	V
SVR	Supply voltage rejection	$f = 100 \text{ Hz to } 10\text{kHz}$	$C_{REF} = 0$		74		dB
			$C_{REF} = 5\mu\text{F}$		86		
$\Delta V_O / \Delta T$	Output voltage drift					150	ppm/ $^\circ\text{C}$
I_{SC}	Output current limit	$R_{SC} = 10\Omega, V_O = 0 \text{ V}$			65		mA
V_I	Input voltage range			9.5		40	V
V_O	Output voltage range			2		37	V
$V_O - V_I$				3		38	V
I_d	Quiescent current	$V_I = 30\text{V}, I_O = 0 \text{ mA}$			2.3	5	mA
K_{VH}	Long term stability				0.1		%/1000 hrs
eN	Output noise voltage	BW = 100 Hz to 10 kHz	$C_{REF} = 0$		20		μV
			$C_{REF} = 5\mu\text{F}$		2.5		

Table 5. Electrical characteristics for LM723C (refer to the test circuits, $T_A = 25^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$\Delta V_O/\Delta V_I$	Line regulation	$V_I = 12 \text{ to } 15 \text{ V}$			0.01	0.1	%
		$V_I = 12 \text{ to } 40 \text{ V}$			0.1	0.5	
		$V_I = 12 \text{ to } 15 \text{ V}, T_A = 0 \text{ to } 70^\circ\text{C}$				0.3	
$\Delta V_O/V_O$	Load regulation	$I_O = 1 \text{ to } 50 \text{ mA}$			0.03	0.2	%
		$I_O = 1 \text{ to } 10 \text{ mA}, T_A = 0 \text{ to } 70^\circ\text{C}$				0.6	
V_{REF}	Reference voltage	$I_{REF} = 160 \mu\text{A}$		6.8	7.15	7.5	V
SVR	Supply voltage rejection	$f = 100 \text{ Hz to } 10\text{kHz}$	$C_{REF} = 0$		74		dB
			$C_{REF} = 5\mu\text{F}$		86		
$\Delta V_O/\Delta T$	Output voltage drift					150	ppm/ $^\circ\text{C}$
I_{SC}	Output current limit	$R_{SC} = 10\Omega, V_O = 0 \text{ V}$			65		mA
V_I	Input voltage range			9.5		40	V
V_O	Output voltage range			2		37	V
$V_O - V_I$				3		38	V
I_d	Quiescent current	$V_I = 30\text{V}, I_O = 0 \text{ mA}$			2.3	4	mA
K_{VH}	Long term stability				0.1		%/1000 hrs
eN	Output noise voltage	BW = 100 Hz to 10 kHz	$C_{REF} = 0$		20		μV
			$C_{REF} = 5\mu\text{F}$		2.5		

6 Typical performance characteristics

(unless otherwise specified $V_{O(NOM)} = 3.3\text{ V}$)

Figure 4. Maximum output current vs voltage drop Figure 5. Current limiting characteristics

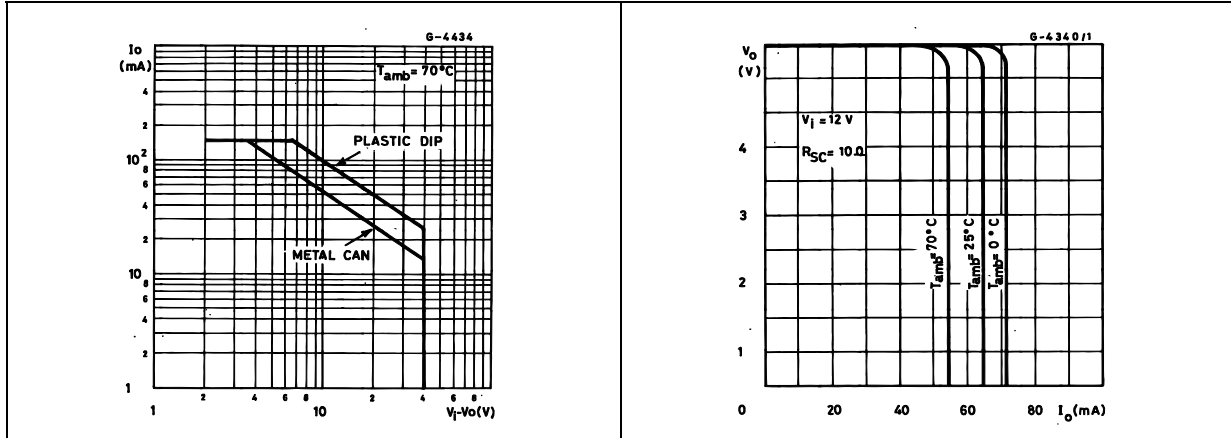


Figure 6. Current limiting characteristics vs junction temperature Figure 7. Load regulation characteristics without current limiting

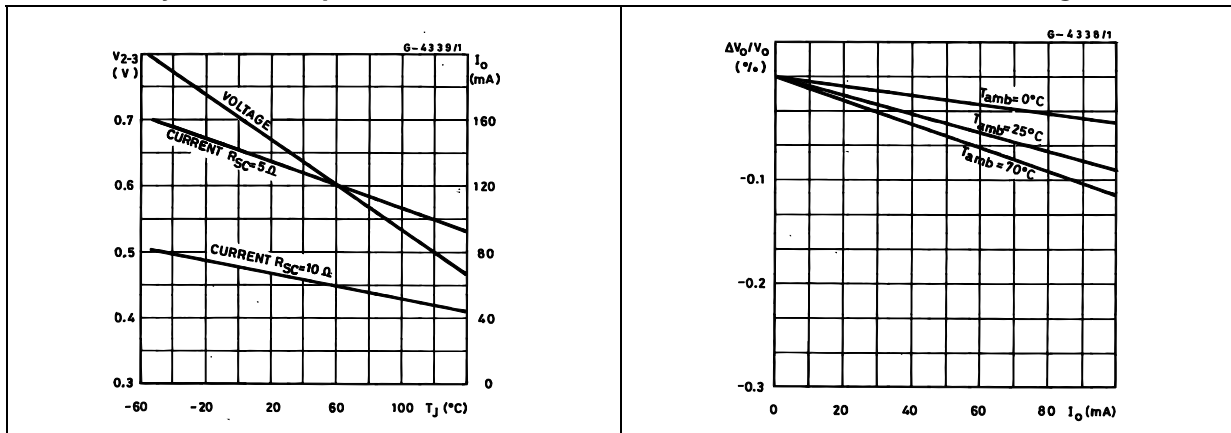


Figure 8. Load regulation characteristics with current limiting Figure 9. Load regulation characteristics with current limiting

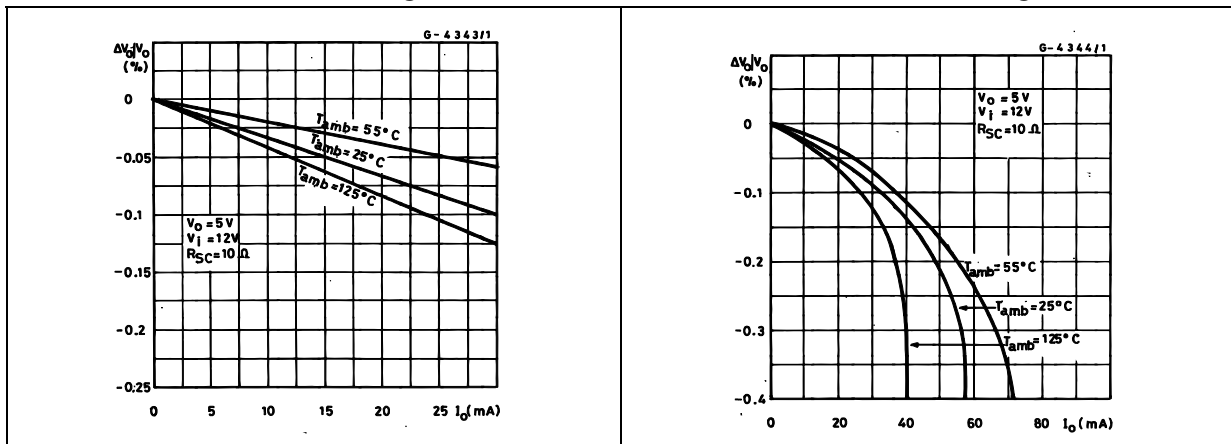


Figure 10. Line regulation vs voltage drop

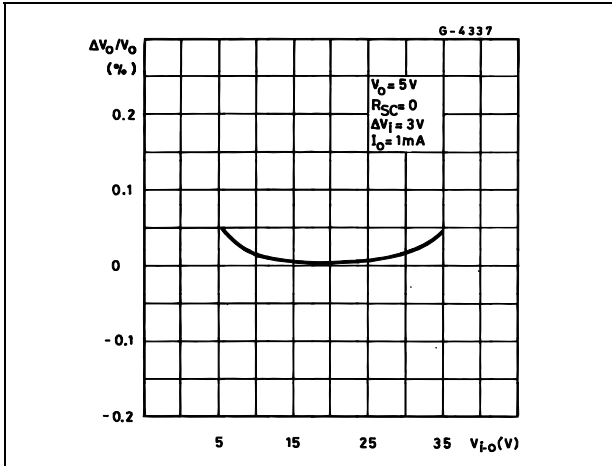


Figure 11. Load regulation vs voltage drop

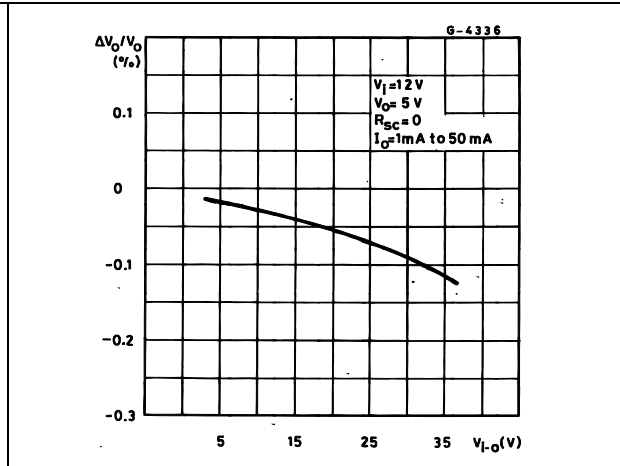


Figure 12. Quiescent drain current vs input voltage

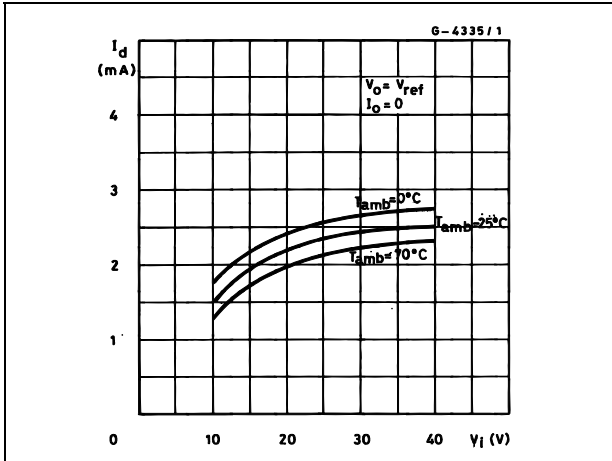


Figure 13. Line transient response

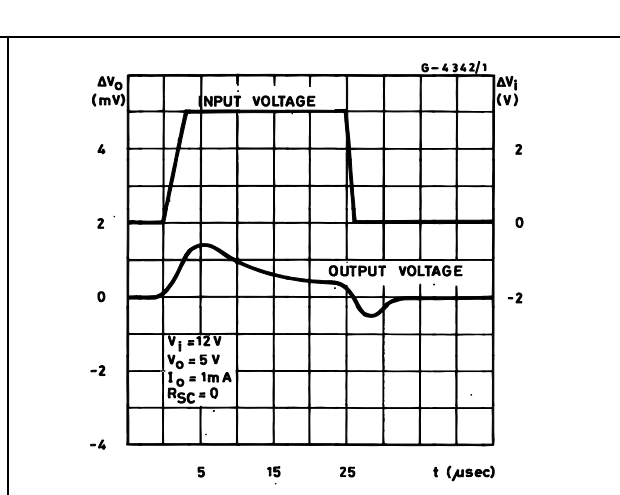


Figure 14. Load transient response

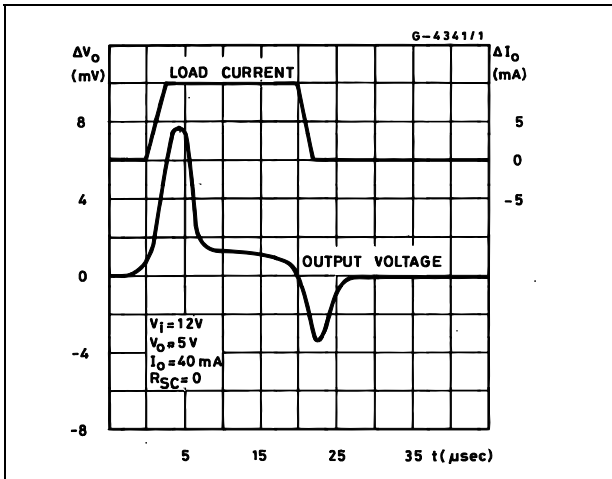


Figure 15. Output impedance vs frequency

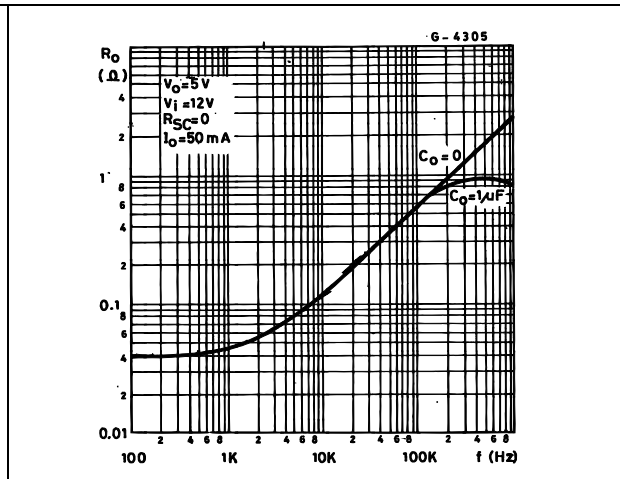


Table 6. Resistor values (kΩ) for standard output voltages

Output Voltage	Applicable figures	Fixed output ± 5%		Output adjustable ± 10% ⁽¹⁾		
		R1	R2	R1	P1	R2
+3	16, 18, 20, 21, 24, 26	4.12	3.01	1.8	0.5	1.2
+5	16, 18, 20, 21, 24, 26	2.15	4.99	0.75	0.5	2.2
+6	16, 18, 20, 21, 24, 26	1.15	6.04	0.5	0.5	2.7
+9	17, 18, 20, 21, 24, 26	1.87	7.15	0.75	1	2.7
+12	17, 18, 20, 21, 24, 26	4.87	7.15	2	1	3
+15	17, 18, 20, 21, 24, 26	7.87	7.15	3.3	1	3
+28	17, 18, 20, 21, 24, 26	21	7.15	5.6	1	2
+45	22	3.57	48.7	2.2	10	39
+75	22	3.57	78.7	2.2	10	68
+100	22	3.57	102	2.2	10	91
+250	22	3.57	255	2.2	10	240
-6 ⁽²⁾	18	3.57	2.43	1.2	0.5	0.75
-9	18	3.48	5.36	1.2	0.5	2
-12	18	3.57	8.45	1.2	0.5	3.3
-15	18	3.65	11.5	1.2	0.5	4.3
-28	18	3.57	24.3	1.2	0.5	10
-45	23	3.57	21.2	2.2	10	33
-100	23	3.57	97.6	2.2	10	91
-250	23	3.57	249	2.2	10	240

1. Replace R1/R2 divider with the circuit of [Figure 27](#).

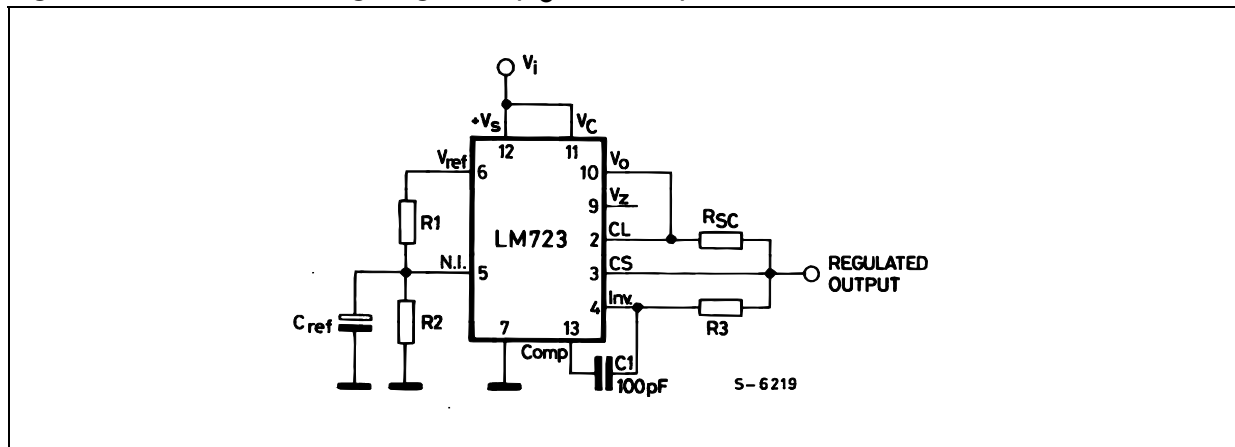
2. V+ must be connected to a +3 V or greater supply.

Table 7. Formula for intermediate output voltages

Conditions		
Outputs from 2 to 7V Figure 16, 19, 20, 21, 24, 26 $V_O = (V_{REF} \times R_2) / (R_1 + R_2)$	Outputs from 4 to 250V Figure 22 $V_O = (V_{REF}/2) \times [(R_2 - R_1)/R_1] ; R_3 = R_4$	Current Limit $I_{LIMIT} = V_{SENSE} / R_{SC}$
Outputs from 7 to 37V Figure 17, 19, 20, 21, 24, 26 $V_O = V_{REF} \times [(R_1 + R_2)/R_2]$	Outputs from -6 to -250V Figure 18, Figure 23 $V_O = (V_{REF}/2) \times [(R_1 + R_2)/R_1] ; R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [(V_O \times R_3) / (R_{SC} \times R_4)] \times [V_{SENSE} \times (R_3 + R_4)] / (R_{SC} \times R_4)$ $I_{SHORTCKT} = (V_{SENSE} / R_{SC}) \times [(R_3 + R_4) / R_4]$

7 Applications information

Figure 16. Basic low voltage regulator ($V_O = 2$ to 7 V)



Note: $R_3 = (R_1 \times R_2) / (R_1 + R_2)$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

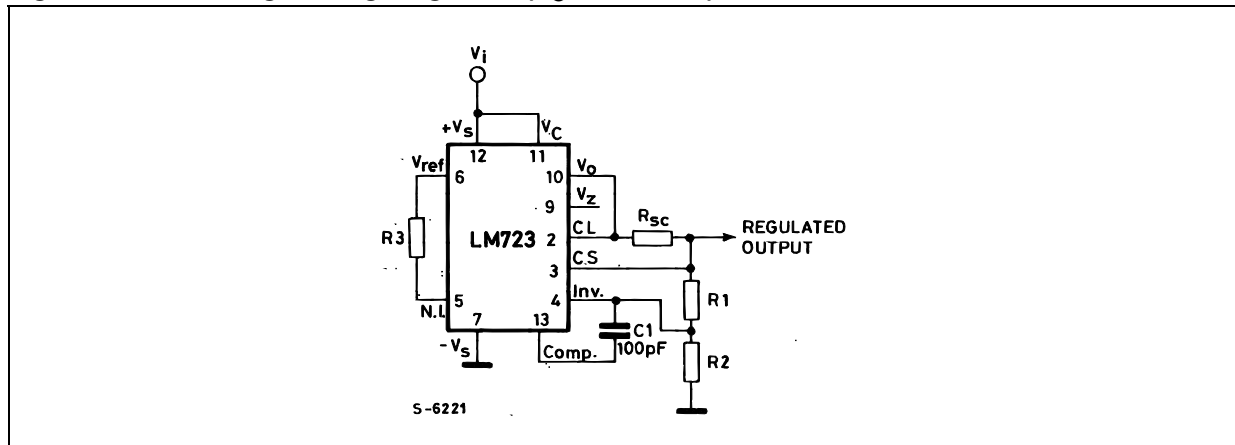
Typical performance

Regulated output voltage.....5 V

Line regulation ($\Delta V_I = 3$ V).....0.5 mV

Load regulation ($\Delta I_O = 50$ mA)....1.5 mV

Figure 17. Basic high voltage regulator ($V_O = 7$ to 37 V)



Note: $R_3 = (R_1 \times R_2) / (R_1 + R_2)$ for minimum temperature drift.

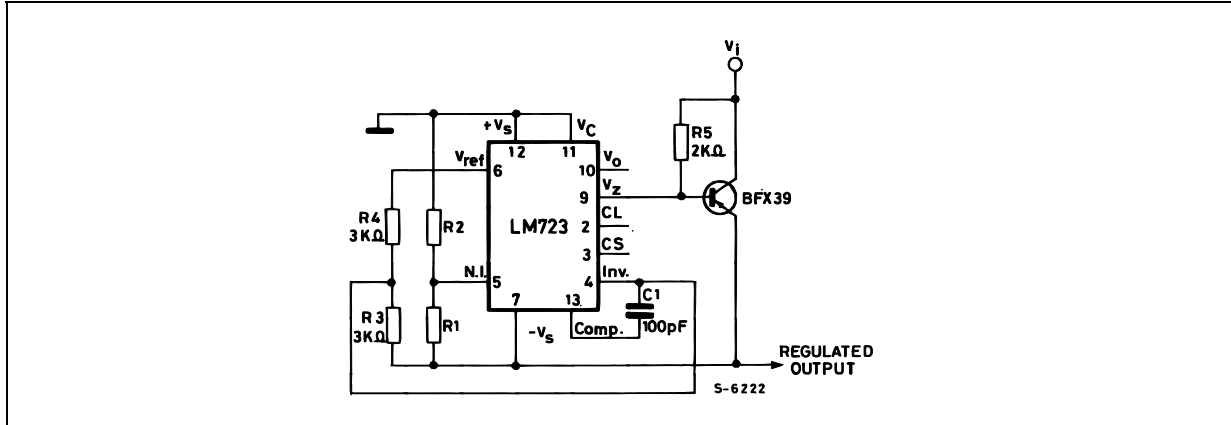
R_3 may be eliminated for minimum component count.

Typical performance

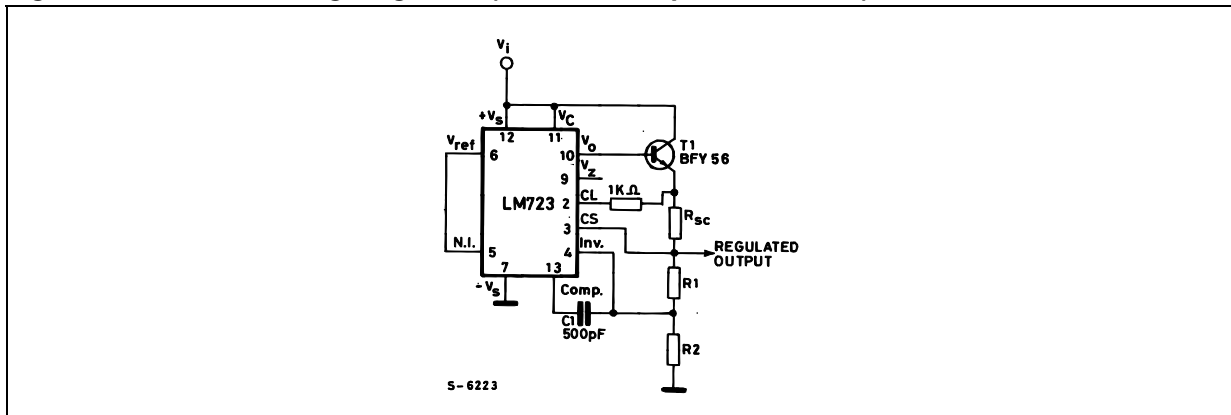
Regulated output voltage.....15 V

Line regulation ($\Delta V_I = 3$ V).....1.5 mV

Load regulation ($\Delta I_O = 50$ mA).....4.5 mV

Figure 18. Negative voltage regulator

Note: Typical performance
 Regulated output voltage.....15 V
 Line regulation ($\Delta V_I = 3\text{ V}$).....1 mV
 Load regulation ($\Delta I_O = 100\text{ mA}$).....2 mV

Figure 19. Positive voltage regulator (external NPN pass transistor)

Note: Typical performance
 Regulated output voltage.....15 V
 Line regulation ($\Delta V_I = 3\text{ V}$).....1.5 mV
 Load regulation ($\Delta I_O = 1\text{ A}$).....15 mV

The diagram shows a precision current source circuit. An input voltage V_i is connected to the non-inverting input (pin 11) of the LM723 through a resistor R_3 (60 Ω). The LM723 is configured with its inverting input (pin 10) connected to the output (pin 1) through a feedback resistor of 1 K Ω . The output of the LM723 (pin 1) drives the base of a 2N5001 transistor (T1). The emitter of T1 is connected to ground through a resistor R_{SC} . The collector of T1 is connected to the input voltage V_i through a resistor R_3 . The LM723 is powered by a positive supply $+V_s$ (pin 12) and a negative supply $-V_s$ (pin 13). A reference voltage V_{ref} is applied to pin 6 through resistor R_1 , and a reference capacitor C_{ref} is connected to pin 5. A compensation capacitor C_0 is connected to pin 4. The output of the circuit is the regulated current through R_{SC} , labeled "REGULATED OUTPUT".

Figure 21. Foldback current limiting

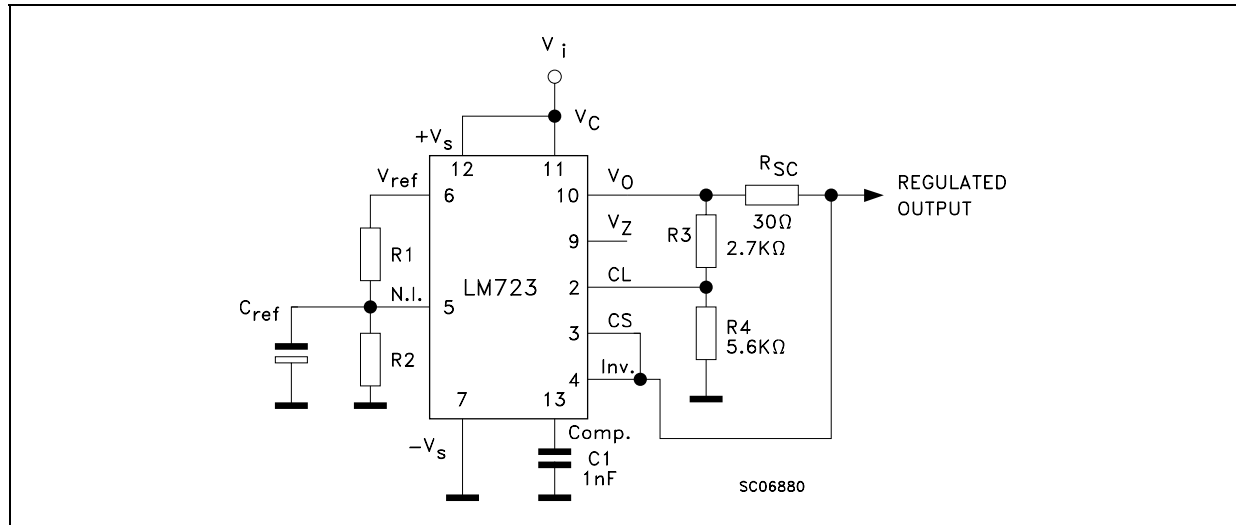
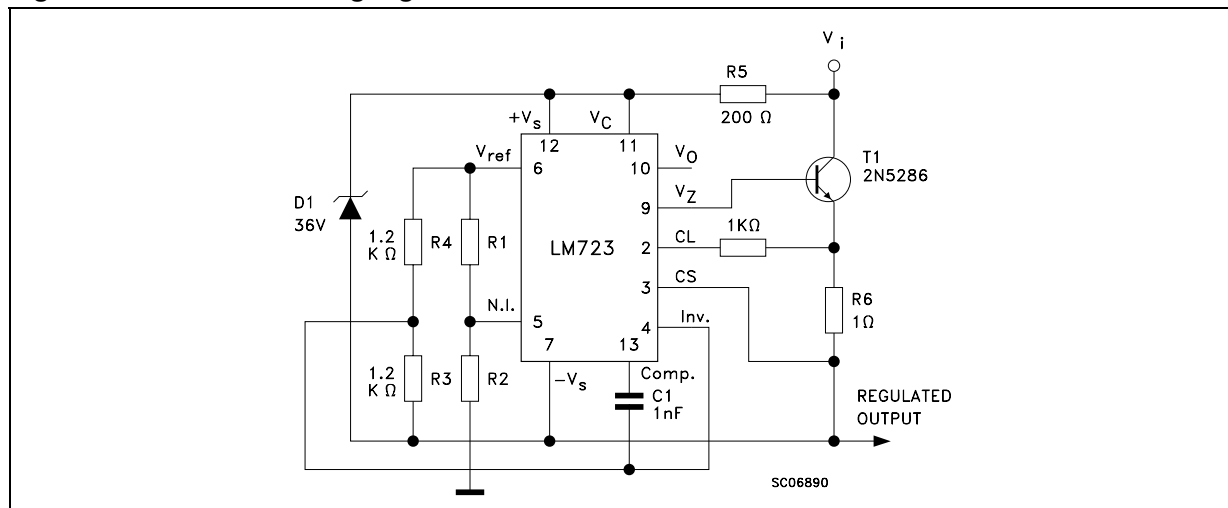


Figure 22. Positive floating regulator



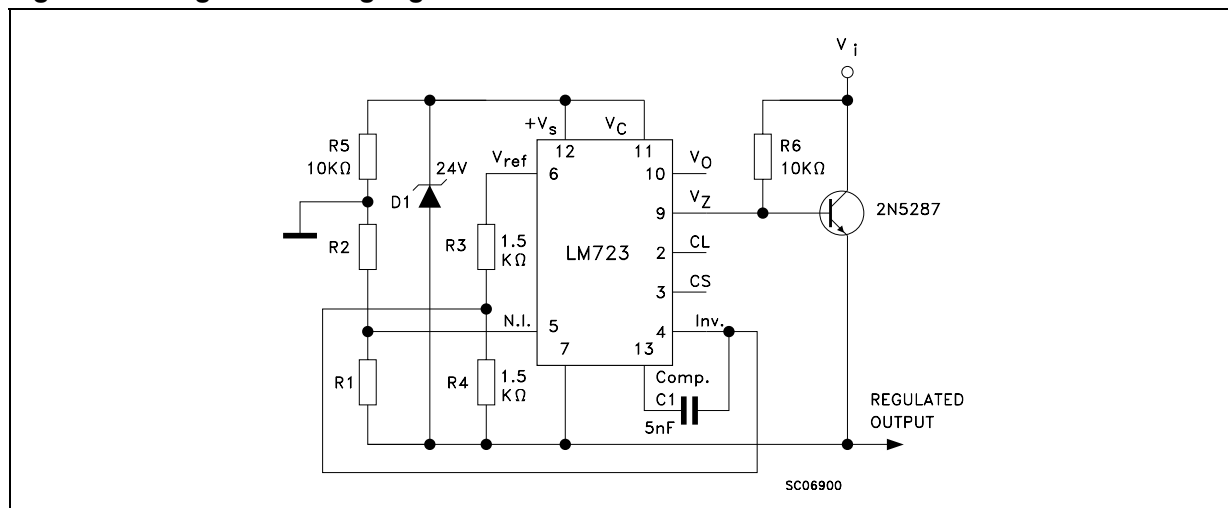
Note: Typical performance

Regulated output voltage.....100 V

Line regulation ($\Delta V_I = 20 V$).....15 mV

Load regulation ($\Delta I_O = 50 mA$).....20 mV

Figure 23. Negative floating regulator



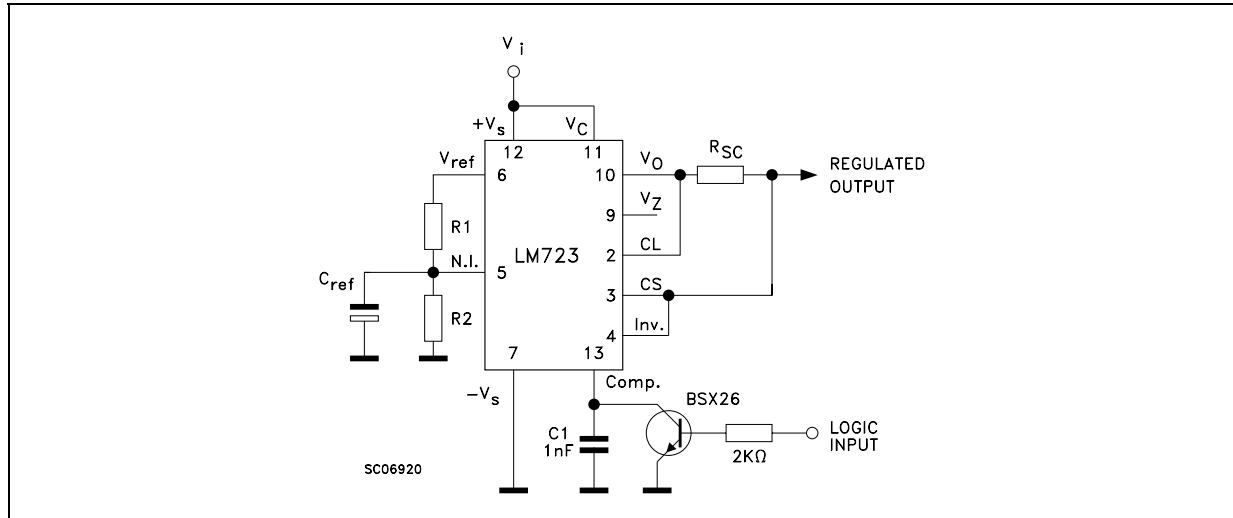
Note: Typical performance

Regulated output voltage.....-100 V

Line regulation ($\Delta V_I = 20 V$).....30 mV

Load regulation ($\Delta I_O = 100 mA$).....20 mV

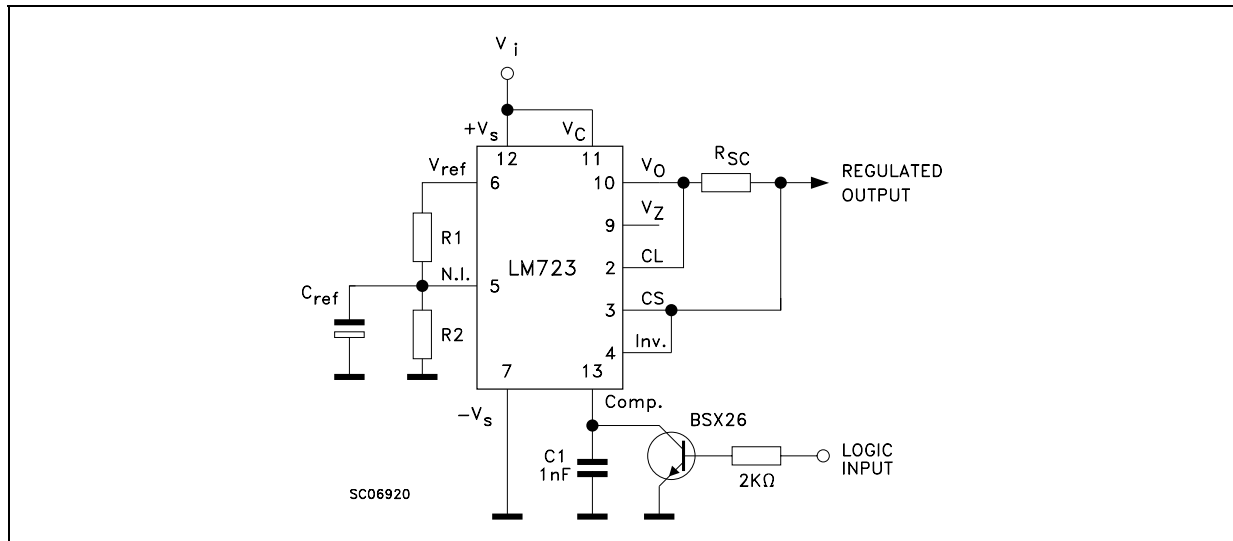
Figure 24. Positive switching regulator



Note: Typical performance

Regulated output voltage.....	5 V
Line regulation ($\Delta V_I = 30 \text{ V}$).....	10 mV
Load regulation ($\Delta I_O = 2 \text{ A}$).....	80 mV

Figure 25. Remote shutdown regulator with current limiting

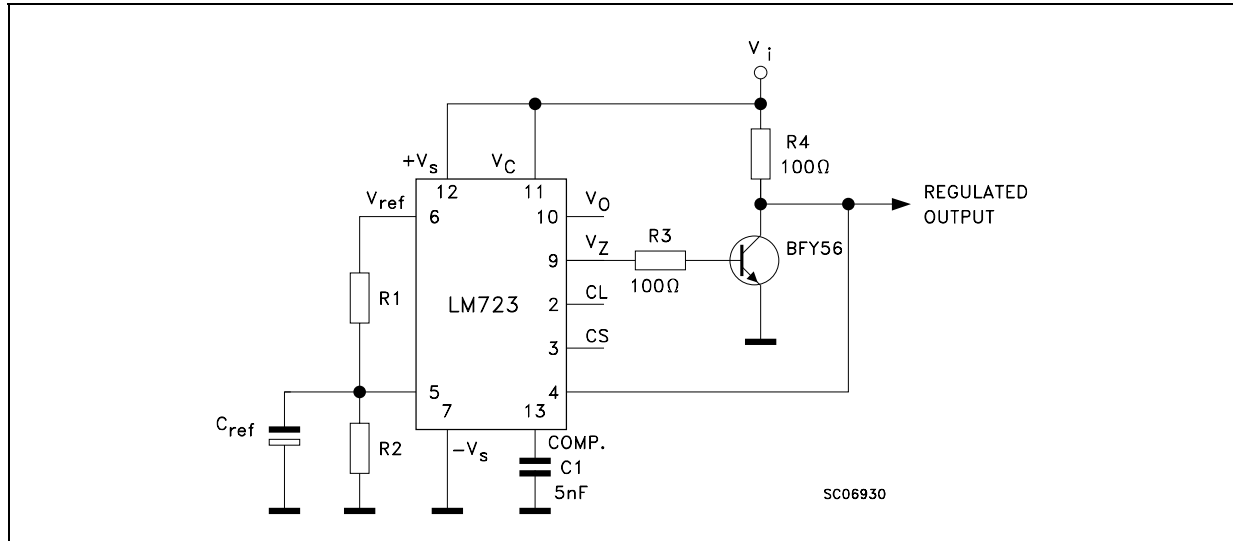


Note: Current limit transistor may be used for shutdown if current limiting is not required.

Typical performance

Regulated output voltage.....	5 V
Line regulation ($\Delta V_I = 3 \text{ V}$).....	0.5 mV
Load regulation ($\Delta I_O = 50 \text{ mA}$).....	1.5 mV

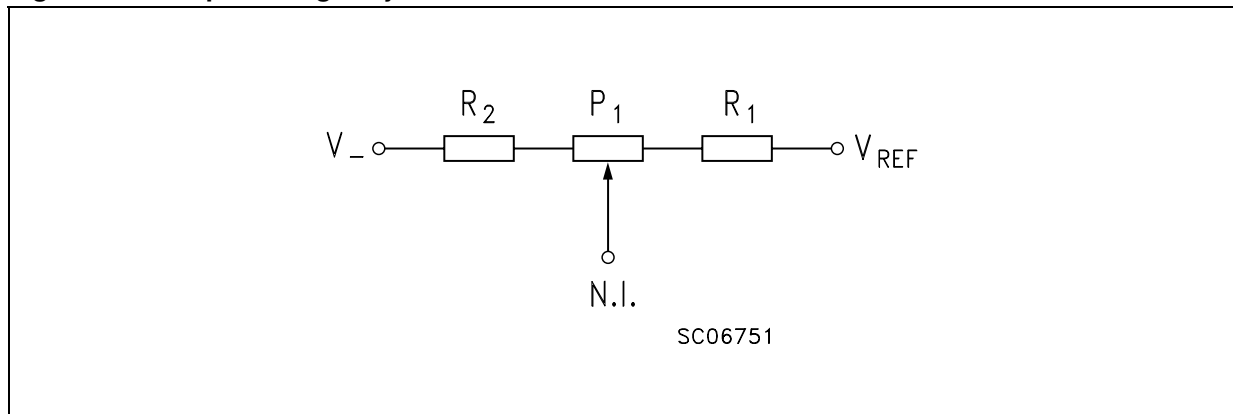
Figure 26. Shunt regulator



Note: Typical performance

Regulated output voltage.....	5 V
Line regulation ($\Delta V_I = 10\text{ V}$).....	2 mV
Load regulation ($\Delta I_O = 100\text{ mA}$).....	5 mV

Figure 27. Output voltage adjust

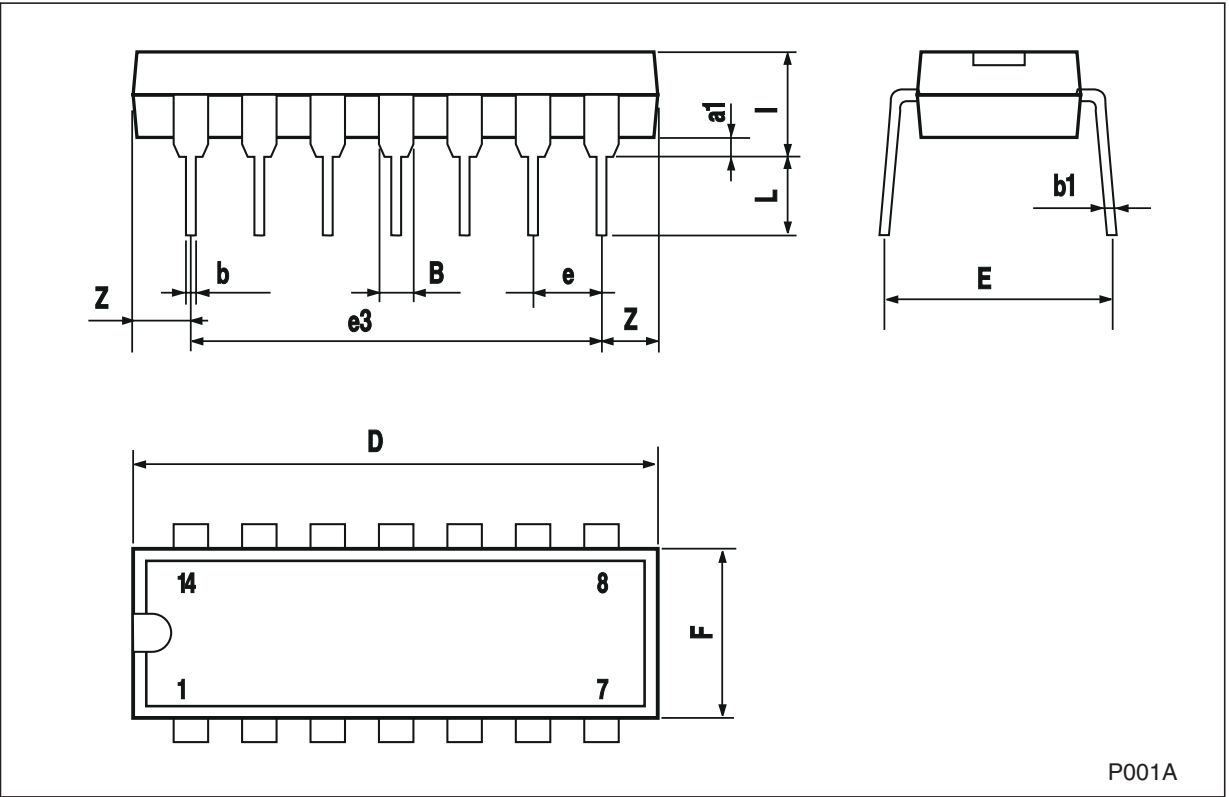


8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Plastic DIP-14 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



9 Revision history

Table 8. Document revision history

Date	Revision	Changes
21-Jun-2004	5	
22-Nov-2007	6	Added Table 1 .

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