1100СК2, К1100СК2, КР1100СК2 Monolithic Sample-and-Hold Circuits

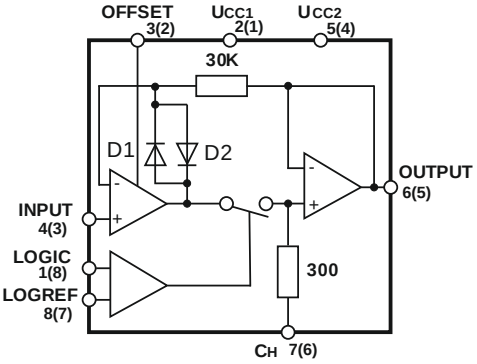
FEATURES

- Supply voltages ±15V (group B), ±12B (group A)
- Less than 7 μs sampling time with an error of 0.1% at C_H = 1000 pF
- Less than 180 ns aperture delay
- Range of input voltages ± 10V (group B), ± 5V (group B)
- External hold capacitor
- Output short-circuit protection
- Compatibility with control input with TTL / CMOS logic

APPLICATIONS

- Ramp generators with variable reset level
- Integrators with programmable reset level
- Synchronous correlators
- 2-Channel switches
- DC and AC zeroing
- Staircase generators

Fig.1 FUNCTIONAL DIAGRAM
Numbering of pins – for 1100СК2, in parentheses - for КР1100СК2



DESCRIPTION

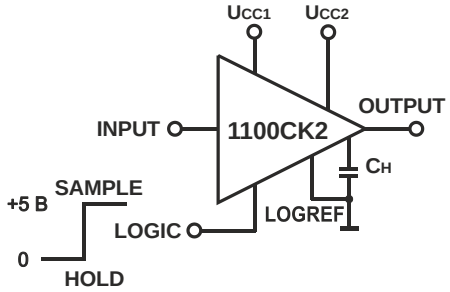
The 1100СК2, К1100СК2, КР1100СК2 are monolithic sample-and-hold (SHA) circuits, controlled by signal LOGIC, stores the instantaneous values of the input signal and for a certain time maintain a constant DC voltage at the output with a high accuracy.

The wide bandwidth allows the 1100СК2 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

The overall design ensures no feedthrough from input to output in the hold mode, even for input signals equal to the supply voltages. Logic inputs on the 1100К2 are fully differential with low input current, allowing for direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4 V. The 1100СК2 will operate from ±5V to ±15V supplies.

The 1100СК2 OUTPUT tracks the INPUT signal by charging and discharging the hold capacitor (C_H). The OUTPUT can be held at any given time by pulling the LOGIC input low relative to the LOGIC REFERENCE voltage and resume sampling when LOGIC returns high. Additionally, the OFFSET pin can be used to zero the offset voltage present at the INPUT.

Fig.2 TYPICAL APPLICATIONS



C_H = 100÷10000 pF

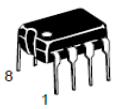
The 1100СК2 and К(КР)1100СК2 devices have a *sample mode* and hold mode controlled by the LOGIC voltage relative to the LOGIC REFERENCE voltage. The device is in *sample mode* when the LOGIC input is pulled high relative to the LOGIC REFERENCE voltage and in *hold mode* when the LOGIC input is pulled low relative to the LOGIC REFERENCE. In *sample* mode, the output is tracking the input signal by charging and discharging the hold capacitor. Smaller values of hold capacitance will allow the output to track faster signals. In *hold mode* the input signal is disconnected from the signal path and the output retains the value on the hold capacitor.

The nominal value of the supply voltage $U_{CC1,2}$=±15V for 1100СК2В и $U_{CC1,2}$=±12V for 1100СК2А, К1100СК2, КР1100СК2.

1100СК2, К1100СК2 are released in ТО5-8, КР1100СК2 in PDIP-8(300Mil).

1100СК2А,В
К1100СК2А,В
ТО5-8

КР1100СК2А,В
PDIP-8



Pin connections

Symbol	Pins number		Description
	TO-5	PDIP-8	
LOGIC	1	8	Logic pin current
U_{CC1}	2	1	Positive supply voltage
OFFSET	3	2	Offset adjust
INPUT	4	3	Analog signal input
U_{CC2}	5	4	Negative supply voltage
OUT	6	5	Analog signal output
CH	7	6	Hold capacitor pin
LOGREF	8	7	Logic reference pin

Fig.3 Representative schematic diagram of input control stage

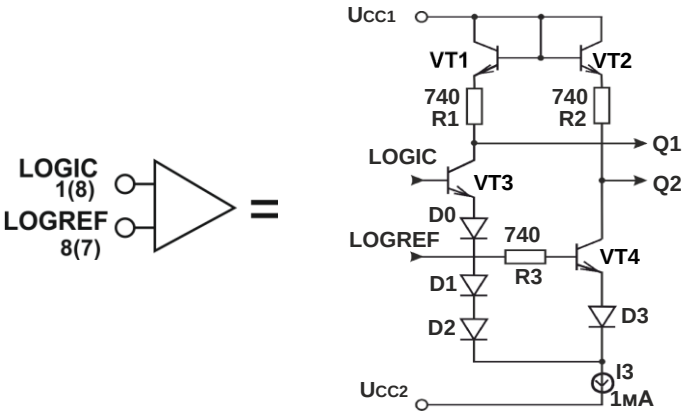


Figure 3 shows a simplified diagram of the input control stage 1100CK2, which explains its operation. The switching threshold of the control signals is set by the voltage drop across the diodes D1, D2 and is approximately 1.4 V. The differential voltage between the LOGIC and LOGREF should be no more than | ± 7V |, and the voltage at these pins must be lower than the positive power supply voltage by 2V and above the voltage of the negative power source by 3V. Signals Q1,Q2 (Fig. 3) controls blocking circuit of the output stage of the first amplifier. In the diagram (Fig. 1), this is shown as a key. This control allows the use of different types and levels of control signals (including analog signals).

Control Configurations

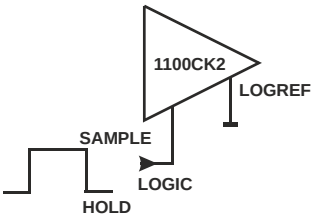


Fig.4 Levels of TTL and CMOS
3V ≤ U_{OH} ≤ 7V, sample - high level,
threshold voltage Uп = + 1,4V**.**

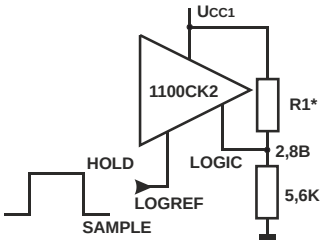


Fig.5 TTL and CMOS levels, sample low, threshold voltage $U_П$ = + 1.4V.
* On the LOGIC pin, set the voltage to 2.8V by selecting the resistance of the resistor R1.

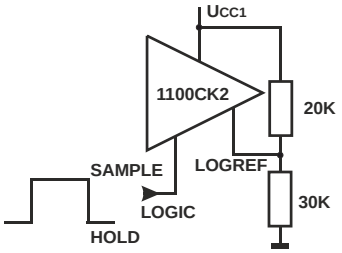


Fig.6 CMOS levels 7V ≤U_{OH} ≤ 15V, high sample, threshold voltage Uп = 0,6U_{CC1} + 1,4V.

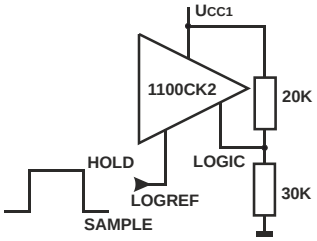


Fig.6 CMOS levels 7V ≤U_{OH} ≤ 15V, high sample, threshold voltage Uп = 0,6U_{CC1} + 1,4V

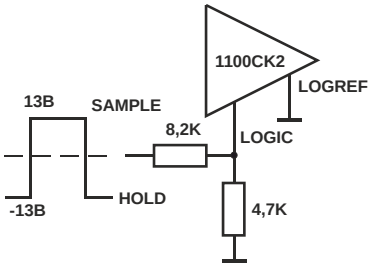


Fig.8 Diagram with divider at the control input, threshold voltage Uп = + 4V.

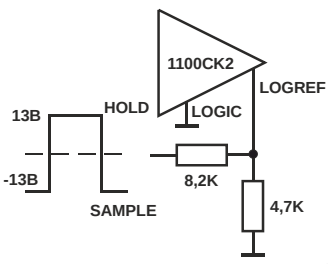


Fig.9 Diagram with divider at the input for setting the threshold, threshold voltage Uп = - 4V.

Electrical Characteristics,

1100CK2B, K(KP)1100CK2B at $U_{CC1,2}$ =±15V; 1100CK2A, K1100CK2A, KP1100CK2A at $U_{CC1,2}$=±12V, T=+25 °C

Parametr, unit	Symbol	1100CK2(A,B)		К1100СК2(А,В) КР1100СК2(А,В)		Test conditions				Notes
		Min	Max	Min	Max	U_{CC1}, V	U_{CC2}, V	U_{IA}, V	U_{ID}, V	
Input offset voltage in sample mode, mV	U_{IO}	-15	15	-15	15	12	-12	0	≥ 3,5	1
				-	-	15	-15			
Offset voltage in hold mode due to charge transfer from the control circuit, mV	U_{IOS}	-20	20	-20	20	12	-12	0	3,5	1
				-	-	15	-15			
Output voltage (amplitude value), V	U_{OA}	0,95U_{IA}	1,05U_{IA}	4,75	5,25	12	-12	± 5	≥ 3,5	1
				-	-	15	-15	± 10		
Supply current, mA	Icc	-	7	-	7	12	-12	0	≥ 3,5	1
					-	15	-15			
Input bias current, nA	I_I	-	200	-	-	12	-12	-	≥ 3,5	1
						15	-15			
Rate of change in output voltage in hold mode , mV/ms.	S_{UOS}	-	2	-	5	12	-12	0	≤ 0,8	1
				-	-	15	-15			
Coefficient of direct transmission of input signal in hold mode, dB	Ks	-	-66	-	- 60	12	-12	± 5	≤ 0,8	1
				-	-	15	-15	± 10		
Sampling time, µs	t_A	-	7	-	10	12	-12	± 5	≥ 3,5	1
				-	-	15	-15	± 10		
Aperture delay, ns	t_{da}	-	180	-	250	12	-12	≥ 2	≥ 3,5	1,2
				-	-	15	-15			

Notes:
1 C_H = 1000 pF ± 2%.
U_{CC1} = 15 V, U_{CC2} = -15 V, R_L = 10 kΩ (for 1100CK2B).
U_{CC1} = 12 V, U_{CC2} = -12 V, R_L = 5 kΩ (for 1100CK2A).
Accuracy of setting and maintaining supply voltages U_{CC} ± 1%.
The resistance R_L is set with an accuracy of ± 5%.
2 Measurement of the aperture delay t_{da} is carried out at SU_{IA} ≤ 3 V / µs.

Maximum permissible operation parameters

Parametr, unit	Symbol	Maximum permissible operation				Absolute Maximum Ratings		Notes
		1100СК2		К1100СК2 КР1100СК2		1100СК2		
		Min	Max	Min	Max	Min	Max	
Power supply voltage is positive polarity, B	U_{CC1}	10,8	13,2	10,8	13,2	6	13,5	Gr. A
		13,5	16,5			6	16,5	Gr. B
Supply voltage negative polarity, B	U_{CC2}	-13,2	-10,8	-13,2	-10,8	-13,5	-6	Gr. A
		-16,5	-10,8			-17	-6	Gr. B
Input voltage, V	U_{IA}	-5	5	-5	5	U_{CC2}+3	U_{CC1}-3	Gr. A
		-10	10			U_{CC2}+3	U_{CC1}-3	Gr. B
Output current, mA	I_O	-	-	-	1	-	-	
Load resistance, kΩ	R_L	5	-	-	-	4	-	Gr. A
		10	-			8	-	Gr. B

Notes:
1 Group A (1100CK2A).
2 Group B (1100CK2B).

RECOMMENDATIONS FOR APPLICATION

1 When working with a microcircuit, precautions should be taken to ensure that static electricity and other voltages do not act on it with the power turned off.

2 It is recommended to apply the mode in the following sequence to the microcircuit:

a) the potential of "earth";

b) supply voltage U_{CC1} = + 15V; U_{CC2} = -15V;

c) voltage to the control inputs LOGIC and LOGREF;

d) input analog voltage.

The procedure for stress relieving must be the reverse.

3 The voltage on the control inputs LOGIC and LOGREF must be below the positive power supply voltage by 2V and above the voltage of the negative power source by 3V. The voltage between these inputs is not higher than | ± 7 | V.

4 The rate of change of the control signal (signal front) must exceed 0.3 V / µs.

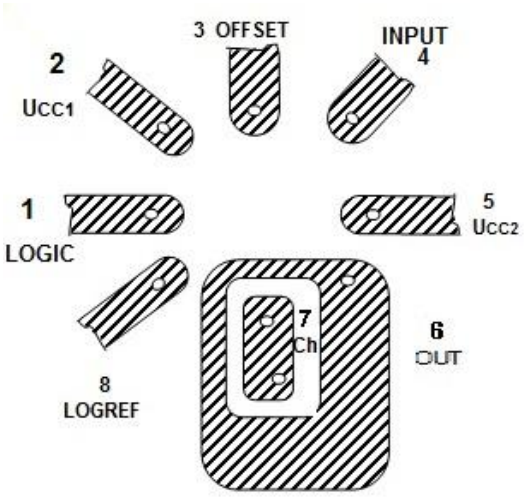
5 It is recommended to use fluoroplastic capacitor of FT-1 type as C_H.

Hold capacitors used in S&H should have a low leakage and guaranteed low dielectric absorption. If the capacitor is charged, then discharged and left to be disconnected from the input circuit, a portion of the previous charge will be restored to it. This phenomenon is called dielectric absorption.

6 The balancing of the circuit using the zero bias voltage in the sampling mode is accomplished by connecting the OFFSET output to a potentiometer with a resistance of 1 kΩ, one terminal of which is connected to the positive pole of the power source, and the second one is grounded through a resistor whose resistance is selected from the condition of passing through the current potentiometer, 6 mA.

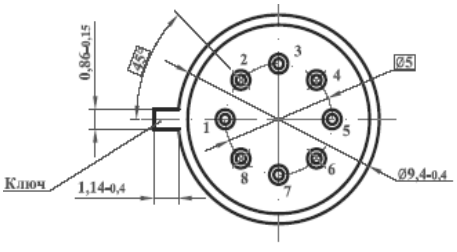
7 To reduce leakage on the board, it is recommended that a printed circuit board with a "guard ring" around the output of the storage capacitor C_H is electrically connected to the output terminal of the chip.

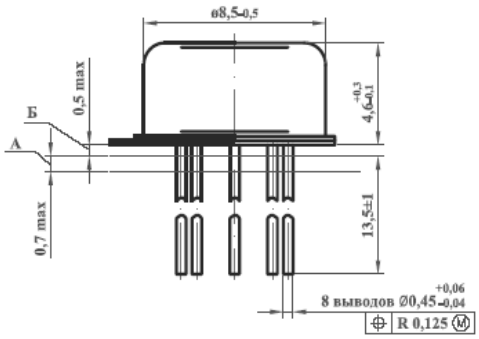
"Guard ring" around the output of hold capacitor (Ch), to reduce leakage across the board



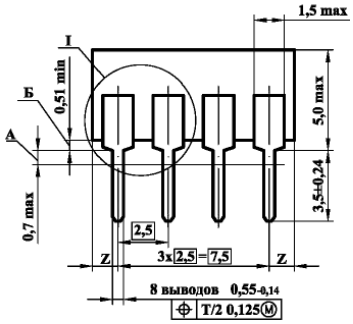
Physical Dimensions in millimeters

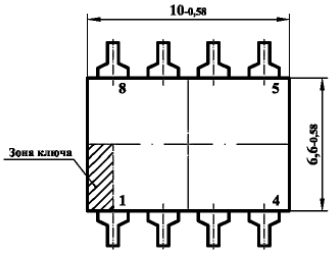
Botton view





8-lead T0-5 metal can package





PDIP-8 (300MIL)